ABSTRACT OF THE INVENTION

A circuit and method is shown for digital control of delay lines in a delay locked loop (DLL) system. A pair of multiplexors (MUXes) is used to select output taps from a pair of complementary delay lines that delay a reference clock signal in order to lock onto a received clock signal. An output tap from one delay line is used to produce a rising edge in an output clock signal while a corresponding tap in the complementary delay line is used to produce a falling edge in the output signal in order to correct for distortion. The MUXes are controlled based on a phase difference detected between the received clock signal and a feedback clock corresponding to the output clock signal. Another aspect of the present invention provides for generation of a quadrature clock by interpolating between the rising and falling edges selected for the output clock signal. Still another aspect of the present invention provides for selectively disabling unused elements of the delay lines to reduce power consumption.

McDonnell Boehnen Hulbert & Berghoff
300 S. Wacker Drive, Floor 3200
Chicago, IL 60606
312-913-0001